



Flexible electronic/optoelectronic microsystems with scalable designs for chronic biointegration

Enming Song^{a,b}, Chia-Han Chiang^c, Rui Li^{d,e}, Xin Jin^f, Jianing Zhao^g, Mackenna Hill^c, Yu Xia^b, Lizhu Li^h, Yuming Huang^b, Sang Min Won^b, Ki Jun Yuⁱ, Xing Sheng^h, Hui Fang^j, Muhammad Ashrafal Alam^f, Yonggang Huang^{k,l,m}, Jonathan Viventi^c, Jan-Kai Chang^{a,b,1}, and John A. Rogers^{a,b,k,m,n,o,p,q,r,s,1}

^aCenter for Bio-Integrated Electronics, Northwestern University, Evanston, IL 60208; ^bFrederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801; ^cDepartment of Biomedical Engineering, Duke University, Durham, NC 27708; ^dState Key Laboratory of Structural Analysis for Industrial Equipment, Department of Engineering Mechanics, Dalian University of Technology, 116024 Dalian, China; ^eInternational Research Center for Computational Mechanics, Dalian University of Technology, 116024 Dalian, China; ^fSchool of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907; ^gDepartment of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801; ^hDepartment of Electronic Engineering, Tsinghua University, 100084 Beijing, China; ⁱSchool of Electrical and Electronic Engineering, Yonsei University, 03722 Seoul, Republic of Korea; ^jDepartment of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115; ^kDepartment of Mechanical Engineering, Northwestern University, Evanston, IL 60208; ^lDepartment of Civil and Environmental Engineering, Northwestern University, Evanston, IL 60208; ^mDepartment of Materials Science and Engineering, Northwestern University, Evanston, IL 60208; ⁿDepartment of Biomedical Engineering, Northwestern University, Evanston, IL 60208; ^oDepartment of Neurological Surgery, Northwestern University, Evanston, IL 60208; ^pDepartment of Chemistry, Northwestern University, Evanston, IL 60208; ^qDepartment of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL 60208; ^rSimpson Querrey Institute, Northwestern University, Evanston, IL 60208; and ^sFeinberg School of Medicine, Northwestern University, Evanston, IL 60208

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Flexible biocompatible electronic systems that leverage key materials and manufacturing techniques associated with the consumer electronics industry have potential for broad applications in biomedicine and biological research. This study reports scalable approaches to technologies of this type, where thin microscale device components integrate onto flexible polymer substrates in interconnected arrays to provide multimodal, high performance operational capabilities as intimately coupled biointerfaces. Specifically, the material options and engineering schemes summarized here serve as foundations for diverse, heterogeneously integrated systems. Scaled examples incorporate >32,000 silicon microdie and inorganic microscale light-emitting diodes derived from wafer sources distributed at variable pitch spacings and fill factors across large areas on polymer films, at full organ-scale dimensions such as human brain, over ~150 cm². In vitro studies and accelerated testing in simulated biofluids, together with theoretical simulations of underlying processes, yield quantitative insights into the key materials aspects. The results suggest an ability of these systems to operate in a biologically safe, stable fashion with projected lifetimes of several decades without leakage currents or reductions in performance. The versatility of these combined concepts suggests applicability to many classes of biointegrated semiconductor devices.

heterogeneous integration | flexible electronics | bioelectronics | biomedical implants | electrocorticography

Large-scale electronic/optoelectronic platforms that support intimate, functional biointerfaces offer important capabilities in monitoring and/or stimulation of living tissues with relevance to both biological research and clinical therapy (1–7). Emerging classes of flexible biointegrated systems offer many powerful options in this context, as implants for long-term, biologically safe operation (8–13), with examples that range from flexible sheets of electronics for electrophysiological mapping on endo- and epicardial surfaces (14, 15) to thin optoelectronic probes for optical stimulation/recording of neural activity in the depths of the brain (16, 17). An essential feature of such technologies is that they can bend, flex, and twist while in contact with soft, moving biological tissues to minimize damage and to support long-term stable operation. Although approaches based on organic semiconductors, nanowires/particles, and 2D materials are of some interest, those that exploit micro/nanoscale forms of well-established inorganic semiconductors often provide superior levels of functionality and performance, in some cases at levels that compare favorably to those of conventional electronic/

optoelectronic devices built on planar, rigid semiconductor wafers (18–26). The most sophisticated embodiments include arrays of transistors based on silicon nanomembranes (Si-NMs) distributed on shape-conformal sheets, with designs that provide signal amplification and multiplexed addressing at each unit cell across the system (27–29). Here, high quality, thin layers of SiO₂ can serve as flexible biofluid barriers and/or capacitive measurement interfaces (30–32). The dense, defect-free nature of SiO₂ formed by thermal growth on device-grade silicon wafers (referred to here as t-SiO₂) act as remarkably effective barriers across macroscopic areas, with lifetimes projected to extend to many decades, where a slow hydrolysis process causes eventual failure (33, 34).

Although these concepts enable interesting classes of bio-integrated devices, they require custom processing steps, some of which are best suited to academic cleanrooms and manual operation. Schemes that retain these essential ideas, but align with

Significance

Emerging classes of flexible electronic systems designed to interface to soft tissues of the human body serve as the foundations for bioelectronic forms of medicine, with capabilities that can complement those of traditional pharmaceutical approaches. This work establishes the engineering science of categories of biointegrated microsystems that include assemblies of tens of thousands of microdevices interconnected into functional networks on thin flexible polymer substrates with areas that approach those of the human brain. Detailed in vitro studies suggest the ability of these systems to provide sophisticated electronic and optoelectronic function with stable, biologically safe operation for many decades. The results define concepts and technological approaches with widespread utility in the field of bioelectronics.

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¹To whom correspondence may be addressed. Email: jkchang@northwestern.edu or jrogers@northwestern.edu.

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the highly automated manufacturing infrastructure that supports the consumer electronics industry could facilitate broad distribution of similar platforms for use by the research community and, ultimately, for translation to human healthcare. In this context, microscale transfer printing techniques for rapid, parallel delivery of micro/nanomaterials and devices from source wafers to target surfaces are highly relevant, as previously demonstrated with microscale inorganic light-emitted diodes (μ -ILEDs), photodetectors, and piezoelectric microcomponents for use in optogenetics, oximetry, and biopsy (35–37) and, separately, in small collections of complementary metal-oxide–semiconductor (CMOS) microdie (38, 39), with industrially proven uses in photovoltaics, information display, and others.

The results presented here combine and extend these approaches in ways that provide access to deterministic assemblies of large collections of silicon microdie and compound semiconductor μ -ILEDs, both sourced from semiconductor wafers compatible with processing at commercial vendors, but released and distributed in dense and/or sparse arrays on thin flexible polymer substrates. The scales of the demonstrations significantly exceed those of the past publications in terms of overall areas (from ~ 1 to 150 cm^2) (27), numbers of functional elements (from $\sim 2,000$ to $\sim 64,000$) (29), numbers of measurement/stimulation channels (from ~ 300 to $\sim 32,000$), and assembly throughput (from ~ 300 to $>1,000$ microcomponents per printing operation) for applications such as those in neural/cardiac electrophysiology, optogenetics, and optical monitoring (27–29, 35, 37). More generally, the schemes offer a manufacturable route to heterogeneous integration with high registration accuracy at spatially variable densities, layouts, and geometries. Specific examples include interconnected electronic–optoelectronic microsystems that exploit thin printable microdie and μ -ILEDs as pixelated functional components, illustrating concepts for building combined electronic/optoelectronic systems in thin/flexible formats. Cointegration with $t\text{-SiO}_2$ biofluid barriers yields long-term stability, over timeframes that project to many decades of immersion in simulated biofluid environments. Performance evaluations, yield studies, accelerated immersion tests, temperature-dependent *in vitro* measurements, and related theoretical simulations highlight the key features. These ideas have potential to serve as the basis of long-lived, highly functional semiconductor device interfaces to living organisms, of particular relevance to neural and cardiac systems.

Results and Discussion

High Speed, Deterministic Assembly of Electronic/Optoelectronic Microdie. As illustrated in previous publications (40–42), powerful classes of large-area, flexible electronic microsystems can be realized by combining conventional electronic materials and microfabrication processes with transfer printing techniques. Here, the transfer process allows for rapid, deterministic manipulation and assembly of microdie released from fully processed semiconductor wafers with advanced undercut etching techniques. The results can yield large-scale arrays in arbitrary layouts over large areas on substrates of interest in ambient conditions. Fig. 1*A* presents a schematic illustration and optical micrographs of advanced implementations of this scheme, starting with 1) controlled release of silicon CMOS microdie via a combination of reactive ion etching (RIE) and wet chemical etching to form freely suspended arrays tethered to an underlying wafer by thin, narrow bridges that serve as anchors; 2) selective retrieval, *i.e.*, “inking” (43), of selected collections of these microdie onto the patterned surface of an elastomeric stamp; and 3) aligned transfer of these components by contact printing onto a substrate of interest. In this study, each microdie includes a pair of *n*-channel metal-oxide–semiconductor transistors (channel length $L = 10 \text{ }\mu\text{m}$, width $W = 33 \text{ }\mu\text{m}$, silicon thickness of 100 nm) released after fabrication on a silicon-on-insulator (SOI) wafer ($1\text{-}\mu\text{m}$ -thick buried-oxide [BOX] layer). These microdie serve effec-

tively as pixelated electronic components that yield functional microsystems upon electrical interconnection. Detailed information appears in *SI Appendix, Fig. S1*.

Similar to previously reported methods (38, 39), the engineering schemes for creating printable silicon microdie utilize photolithography and inductively coupled plasma reactive ion etching (ICP-RIE) through the BOX layer at the periphery of each microdie (Fig. 1*A*) to establish trenches that expose the underlying Si wafer. Undercut release follows from anisotropic etching of the wafer by immersion in a bath of tetramethylammonium hydroxide (TMAH, 8.3%). Here, a bilayer of $\text{SiO}_2/\text{SiN}_x$ ($1 \text{ }\mu\text{m}/600 \text{ nm}$) formed by plasma-enhanced chemical-vapor deposition (PECVD) at $350 \text{ }^\circ\text{C}$ encapsulates the front side of the microdie as protection from exposure to TMAH. The released microdie remain tethered to their original locations in freely suspended forms joined to the underlying wafer by anchor structures of SiN_x ($15 \times 100 \text{ }\mu\text{m}^2$, 600-nm thick), while the BOX layer serves as an etch stop and backside protection. Detailed information on microdie architecture appears in *SI Appendix, Fig. S2*, where the dimensions are $220 \times 150 \times 3 \text{ }\mu\text{m}$.

Retrieval of selected sets of these suspended microdie occurs with stamps of poly(dimethylsiloxane) (PDMS) with relief features and spacings matched to the sizes and layouts of the microdie. Specifically, an automated system provides precise alignment and control over contact for the selective inking process. The anchors fracture mainly as a result of pressure associated with contact to stamp, such that retraction of the stamp leaves collections of microdie weakly bonded by van der Waals forces to the surface of the PDMS. Printing of the microdie “inks” onto a target substrate yields heterogeneously integrated systems. In examples reported here, a coating of a low-modulus polymer (Intervia photodielectric 8023; $\sim 2 \text{ }\mu\text{m}$) serves as an adhesive to ensure nearly 100% yields in transfer, reproducibly. Multiple cycles of this printing process, conducted in a step and repeat fashion, can yield distributed arrays of microdie over areas that are much larger than those of the original SOI wafer. For plastic substrates, the resulting systems offer excellent degrees of bendability, particularly for thin microdie configured to lie near the neutral mechanical plane by use of overcoats with suitable thicknesses, without adverse effect on the performance characteristics. The electrical properties of representative transistors (on/off ratio $\sim 10^7$, mobility $\sim 600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and threshold voltage $[V_T] \sim 1 \text{ V}$) are in *SI Appendix, Fig. S3*.

Fig. 1*B–D* present a series of optical micrographs of a PDMS stamp after retrieval of a collection of microdie, captured at various levels of magnification (from left to right). This example involves $\sim 1,000$ microdie distributed over an area of $1.5 \times 1.5 \text{ cm}^2$ on the surface of a stamp ($100\text{-}\mu\text{m}$ relief and 4-mm -thick substrate; Fig. 1*B*). As in Fig. 1*C*, an automated tool allows for alignment and registration with positioning accuracy of $\sim 1 \text{ }\mu\text{m}$. Fig. 1*D* shows magnified side (scanning electron microscope [SEM] image), bottom, and top views (optical micrographs) of a representative microdie ($\sim 3\text{-}\mu\text{m}$ thick) on the raised features of relief on the stamp. Careful control of the release and transfer mechanics enables manipulation of large-scale arrays with high throughput, as in Fig. 1*E*. Here, 2 SEM images (Fig. 1*E*, *Left* and *Right*) highlight different areas across a processed SOI wafer (Fig. 1*E*, *Middle*, optical image) before and after selective retrieval, showing freely suspended microdie arrays tethered by SiN_x anchors and their removal, respectively.

Fig. 1*F* and *G* feature the architecture of a microdie released from the source wafer and after transfer printing. The schematic illustration of the cross-sectional undercut profile (Fig. 1*F*) includes the structures and thicknesses of the different layers. The SEM and profilometry images (Fig. 1*G*) in sequence show the released/printed structure ($\sim 3 \text{ }\mu\text{m}$) and undercut profile, where the sidewall angle of 54.7° results from the anisotropic etching process. Here, the $\text{SiO}_2/\text{SiN}_x$ ($1 \text{ }\mu\text{m}/600 \text{ nm}$) bilayer on top has

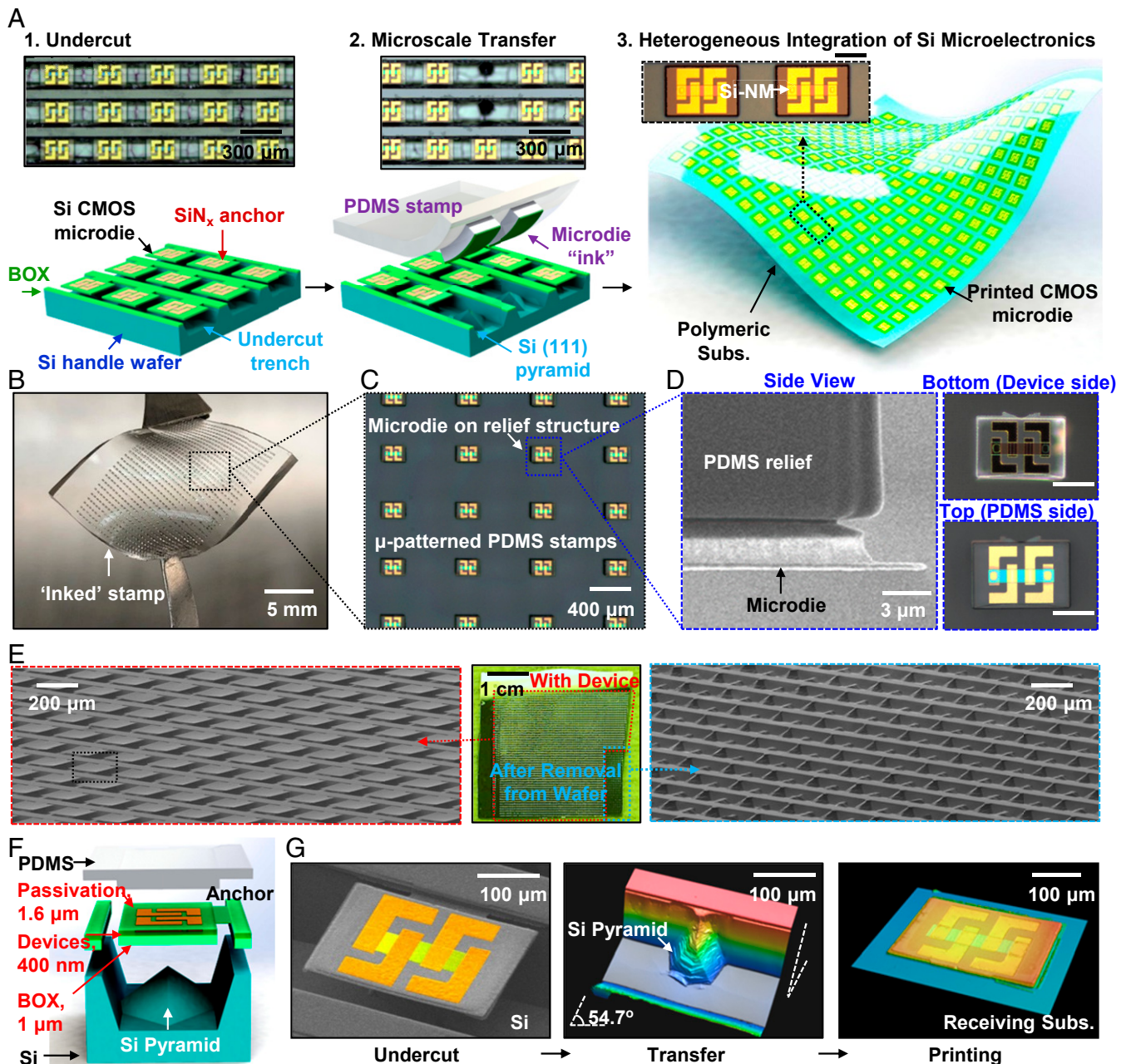


Fig. 1. Scalable approaches for deterministic assembly of semiconductor microdevices into flexible systems for biointegration. (A) Processing schemes for printing of flexible silicon microdie: 1) Formation of trenches on a wafer substrate; 2) retrieval with a PDMS stamp; and 3) printing on a polymeric substrate. *Insets* are optical images of arrays of microdie on a source wafer before/after transfer, and silicon microdie printed onto a receiving substrate (scale bar, 100 μm). (B) Photographs of a PDMS stamp inked with ~1,000 microdie. (C) Magnified image of an array of microdie on a PDMS stamp. (D) SEM and optical images of an inked PDMS stamp in side, bottom, and top views (scale bar, 100 μm). (E, *Left*) SEM image of a large array of microdie released from the source wafer after undercut etching. (E, *Middle*) Photograph of an entire source wafer. Red and blue frames correspond to areas with and without released arrays of microdie, respectively. (E, *Right*) SEM image of an etched structure after complete removal of an array of microdie. (F) Schematic illustration of the material stack layout and thicknesses of the different layers at the location of a microdie after complete release. (G) A group of SEM and optical profilometry images shown in sequence for a representative unit cell after undercut, after removal and after printing onto a target substrate. The undercut angle in the silicon is 54.7°, consistent with the anisotropic behavior of the etchant.

internal stresses that balance those of the released microdie, thereby eliminating any significant bowing.

Transfer Printing of Microdie Arrays at Variable Densities. Fig. 2 demonstrates other key features that follow from a transfer-printing approach to heterogeneous integration. Engineering the distribution of patterned relief structures on the stamps

creates efficient routes to assemblies of microdie at variable densities and layouts, with increasing versatility as the number of relief features decreases and the number of step and repeat cycles of printing increases. The schematic illustrations in Fig. 2A highlight examples, where dense arrays of relief structures compose the letter “N” with sparse distributions in the background regions. Fig. 2, *Insets*, are optical images of corresponding relief

100 × 110 μm or 350 × 440 μm in a geometry suggestive of demands for spatial resolution in electrical mapping or stimulation of different sensory functions in the brain, as a conceptual demonstration of the possibilities. Specifically, the regions of dense distribution (100 × 110 μm) correspond to the locations of primary sensory cortex for visual, auditory, somatic, gustation, and olfactory sensory functions. The sparse distributions appear in motor areas responsible for control of voluntary movements. Such high-definition networks of active electronics have potential relevance in monitoring of electrophysiological activity associated with microseizures and microscale discharges of neurons in the brain in ways that could complement traditional microelectrocorticography (44, 45) by significantly increasing the total number and density of addressable channels with local amplification and active multiplexed schemes for addressing. Fig. 2*B*, *Insets*, show collections of microdie at different levels of magnification, where the optical images highlight the hybrid distribution at the boundaries between sparse/dense arrays (Fig. 2*B*, *Upper*) and include magnified views for local sparse (Fig. 2*B*, *Middle*, blue frame), and dense (Fig. 2*B*, *Lower*, black frame) regions. Fig. 2*C* shows such a system while bending to a radius of curvature at ~3 cm, indicating mechanical flexibility sufficient for conforming to large-scale features of the brain and other soft tissue systems. A statistical analysis of printing yield, defined as the percentage of functional microdie, indicates values >96% for transfer of 256 microdie, or more, in a single operation. Printing failures correspond mainly to fractured/twisted devices (*SI Appendix*, Fig. S4) or associated dislocations. These sorts of defects can be reduced by use of composite stamp designs, frequent cleaning of the stamps, careful control of printing kinetics, and/or operation in an environment with reduced levels of dust/debris (42, 46–48).

Envisioned applications of this printed, large-scale electronic network include shape-conformal bioelectronic interfaces for neural recording or stimulation, configured for mapping on dynamic, curved surfaces of tissues. Fig. 2*D* schematically illustrates contact on a brain model, where the dense arrays align with locations of primary sensory cortex (red highlight). Cointegration of electrode arrays (Au, 300 × 300 μm², 300-nm thick; Fig. 2*E*) and interconnection traces (Fig. 2*E*, *Inset*) yields functional systems with multiplexing capabilities for efficient capture of spatiotemporal patterns of electrical activity with a dramatically reduced number of addressing wires compared with that required for otherwise similar arrays in passive designs, without microdie. Fig. 2*F* summarizes statistical results for the peak effective mobility (μ_{eff}), V_T , and the on/off ratios of 300 representative transistors in printed microdie, derived from standard field effect transistor models (*SI Appendix*) (45). The results suggest excellent uniformity and consistency in the performance across the system.

Integration of Electronic/Optoelectronic Microsystems with Biofluid Barriers of t-SiO₂. A fundamental challenge in the development of flexible electronic systems for applications in biology is that their operational lifetimes are often limited by biofluid ingress. Encapsulation strategies (49) that rely on titanium (50) or ceramic (51) enclosures are effective for electronic implants that do not require mechanical bendability or intimate interfaces with biology, but they are unsuitable for the types of systems envisioned in biointegrated device research or in bioelectronic medicines, for instance. A recently developed approach that avoids limitations associated with coatings deposited or cast over preformed electronics exploits thin layers (submicron thick) of SiO₂ (t-SiO₂) thermally grown on the surfaces of device-grade silicon wafers (32). Here, the t-SiO₂ serves as an encapsulation layer that forms first, followed by transfer printing of microdie and layer-by-layer fabrication of interlayer dielectrics/interconnects to yield functional, flexible electronics upon casting of a

polymer support and removal of the silicon wafer. Transfer of an additional layer of t-SiO₂ can encapsulate the backside surface of such a system. The encapsulation process (Fig. 3*A*) begins with transfer printing of microdie onto a layer of t-SiO₂ (1 μm) on a silicon wafer, followed by lamination of the printed device onto a separately formed layer of t-SiO₂ (900 nm) with a commercial adhesive (Kwik-sil; World Precision Instruments) on a polymer film/glass plate as a temporary support. Dry etching techniques remove the silicon wafer and terminate at the back surface of the t-SiO₂. Peeling the multilayer stack from the glass plate yields a piece of flexible electronics encapsulated on both sides by t-SiO₂ as long-lived, flexible biofluid barriers. Details appear in *SI Appendix*. Fig. 3*B* presents a photograph of a system that consists of 2 × 2 interconnected array of printed microdie, wrapped around a cylindrical tube to illustrate the high level of mechanical flexibility.

Immersion in phosphate-buffered solution (PBS) at 96 °C and at a pH of 7.4, with a continuous electrical bias (alternating current [a.c.], sine wave, 3 V, 100 Hz) applied between transistor electrodes (source, drain, and gate) and a platinum (Pt) reference probe in PBS (Fig. 3*C*), provides a means for accelerated testing of lifetime at elevated temperatures, as reported in previous studies (31, 52–54). The transfer characteristics of the transistors and the associated leakage current appear in Fig. 3*D* and *E*, respectively. Stable operation occurs throughout ~9 d of immersion, comparable to timescales of over 60 y at physiological temperature (37 °C) based on Arrhenius scaling (30). Similarly, soak testing of t-SiO₂-encapsulated magnesium thin films (200 nm, electron-beam evaporation) in settings and layouts similar to those of the microdie arrays reveals that the failure mechanism is hydrolysis of the t-SiO₂ (~100 nm/d in 96 °C PBS), as shown in *SI Appendix*, Fig. S5.

The encapsulation strategy outlined in Fig. 3*A* is compatible not only with silicon electronics, but also with other types of printable semiconductor devices, such as μ-ILEDs, of relevance for combined electronic–optoelectronic systems that offer advanced capabilities in neuroscience research, for instance. Fig. 3*F* provides an example of this type, with cointegration of indium gallium nitride-based (InGaN) μ-ILEDs and microdie onto a common platform with dual-sided t-SiO₂ encapsulation (900 nm), using previously reported procedures for transistors (38) and μ-ILEDs separately (35). The resultant starburst layout facilitates contact over certain types of nonplanar topography, e.g., here shown on a table-tennis ball with a diameter of 4.5 cm. The optical images show a group of magnified views of an integrated microdie, an entire system, and a printed μ-ILED in on and off states, respectively. As shown in Fig. 3*G*, the performance of the μ-ILED and transistor (Fig. 3*G*, *Inset*) remain unchanged after 10³ cycles of bending into cylindrical shapes with radii of curvature of ~2 cm and after 9 d of immersion in 96 °C PBS.

Printed Microelectronic Assemblies for Multiplexed Electrophysiological Mapping. Integration of printed microdie with t-SiO₂ encapsulation layers serves as the basis of active platforms with multiplexed addressing capabilities in high fidelity, spatiotemporal recording of biopotential distributions across soft tissues, including those of the brain. Fig. 4*A* shows an interconnected array for this purpose. Details of the fabrication process appear in *SI Appendix*, Fig. S6. The overall system includes 64 sensing sites (8 columns, 8 rows, area of ~1 cm²) with active matrix readout, each of which contains a printed microdie (Fig. 4*B*) with 2 underlying Si transistors for multiplexed addressing and local buffering (Fig. 4*B*, *Insets*, and *SI Appendix*, Fig. S7) (45). The encapsulating layer of t-SiO₂ (900 nm) also serves as a dielectric interface to soft tissue for capacitive sensing via coupling to the underlying electrodes and buffer transistor for amplification (32). The other transistor (as multiplexer) allows readout of signal from each pixelated unit in a rapid time sequence controlled by a back-end data acquisition (DAQ) system (*SI Appendix*, Figs. S7 and S8) with a minimal number of

physiological temperature (37 °C), also consistent with projections based on previous measurements of the rate of hydrolysis of t-SiO₂ (~0.04 nm/d in 37 °C PBS) (33, 56). Details of the simulation appear in *SI Appendix, Fig. S14*.

Conclusion

In summary, the results presented here establish a scalable approach for building combined electronic–optoelectronic microsystems with potential to serve as functional interfaces to soft tissues. Demonstrations include deterministic assemblies of as many as tens of thousands (>32,000) of thin, microscale functional elements derived from source wafers, as interconnected networks across areas that approach those of the human brain, where dense layers of silica serve as encapsulation for chronically stable operation in biofluids. Alignment of this scheme with state-of-art technologies in the consumer electronics industry is a critically important feature, not only for high performance operation but also for scaled deployment with spatial diversity and variable densities, layouts, and geometries. Detailed studies highlight the robustness and functionality at the materials and device levels. Additional on-

going work seeks to exploit systems of the type described here as implants for animal studies in brain and cardiac research, with ultimate potential for use as therapeutic devices in humans.

Materials and Methods

Details of fabrication steps, device structures, printing processes, transistor characteristics, encapsulation strategy, procedures for soak tests, and failure mechanism analyses appear the *SI Appendix*. Operation of the multiplexing and DAQ systems, in vitro performance of the active matrix systems, and reactive diffusion modeling and simulations of t-SiO₂ dissolution are also in the *SI Appendix*.

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Flexible Electronic/Optoelectronic Microsystems with Scalable Designs for Chronic Bio-Integration

Enming Song,^{a,b} Chia-Han Chiang,^c Rui Li,^{d,e} Xin Jin,^f Jianing Zhao,^g Mackenna Hill,^c Yu Xia,^b Lizhu Li,^h Yuming Huang,^b Sang Min Won,^b Ki Jun Yu,ⁱ Xing Sheng,^h Hui Fang,^j Muhammad A. Alam,^e Yonggang Huang,^{k,l,m} Jonathan Viventi,^c Jan-Kai Chang,^{a,b,l} and John A. Rogers^{a,b,k,m,n,o,p,q,r,s,l}

^a Center for Bio-Integrated Electronics, Northwestern University, Evanston, IL 60208, United States

^b Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801, United States

^c Department of Biomedical Engineering, Duke University, Durham, NC 27708, United States

^d State Key Laboratory of Structural Analysis for Industrial Equipment, Department of Engineering Mechanics, Dalian University of Technology, Dalian 116024, China

^e International Research Center for Computational Mechanics, Dalian University of Technology, Dalian 116024, China

^f School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, United States

^g Department of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, United States

^h Department of Electronic Engineering, Tsinghua University, Beijing 100084, China

ⁱ School of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, Republic of Korea

^j Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, United States

^k Department of Mechanical Engineering, Northwestern University, Evanston, IL 60208, United States

^l Department of Civil and Environmental Engineering, Northwestern University, Evanston, IL 60208, United States

^m Department of Materials Science and Engineering, Northwestern University, Evanston, IL 60208;

ⁿ Department of Biomedical Engineering, Northwestern University, Evanston, IL 60208;

^o Department of Neurological Surgery, Northwestern University, Evanston, IL 60208;

^p Department of Chemistry, Northwestern University, Evanston, IL 60208;

^q Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL 60208;

^r Simpson Querrey Institute, Northwestern University, Evanston, IL 60208;

^s Feinberg School of Medicine, Northwestern University, Evanston, IL 60208;

¹ To whom correspondence should be addressed. Email: jkchang@northwestern.edu and jrogers@northwestern.edu.

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Supplementary Information

Supplementary Note 1

Supplementary Figure Legends

Supplementary Figure S1-S14

Supplementary Note 1: Materials and Methods

Fabrication of Arrays of Printable Microdie. As shown in *SI Appendix, Fig. S1A*, the fabrication started with formation of isolated silicon transistors on an SOI wafer (100 nm thick device Si, 1 μm thick BOX layer and 500 μm thick handle Si wafer). Solid source doping with phosphorus (at 1000 $^{\circ}\text{C}$ for 10 min) formed source and drain contacts at concentrations of $\sim 10^{19} \text{ cm}^{-3}$, followed by photolithography and reactive ion etching (RIE) with SF_6 to isolate the array of NMOS transistors. Thermal oxidation and atomic layer deposition (ALD) at ~ 1150 $^{\circ}\text{C}$ (16 min) and 80 $^{\circ}\text{C}$ (130 cycles) yielded a dielectric stack of SiO_2 (50 nm) / Al_2O_3 (13 nm). Electron-beam evaporation of Cr/Au (10/300 nm) and photolithographically patterning defined source, drain and gate electrodes. A 1- μm thick layer of SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD, Trion Orion Minilock) served as encapsulation. Photolithography and inductively coupled plasma (ICP)-RIE with SF_6 through the BOX layer yielded isolated microdie blocks, forming trenches into the underlying Si wafers for subsequent undercut etching with TMAH. An additional PECVD layer of SiN_x (Surface Technology System, 600 nm thickness) formed a bilayer encapsulation on top and simultaneously served as the anchor structures, followed with a ICP-RIE step (SF_6) (photolithography defined microdie and anchor), thereby yielding microdie tethered at their original locations via the SiN_x anchors. *SI Appendix, Fig. S1B* shows an optical image of the resulting source wafer (SOI wafer), which involves $\sim 10,000$ microdies. Inset is a representative unit cell with trenches after dry etching. Subsequent wet chemical undercut

etching involved immersion in 8.3% TMAH (at 85 °C in hours), leading to formation of an array of suspended microdie over etched prism shaped trenches in the silicon (depth of ~110 μm). *SI Appendix, Fig. S2* displays an exploded-view schematic illustration of the material stacks for a 4×4 array of released microdie, with thicknesses of each layer. Transfer printing allowed delivery of selected sets of devices from this array onto a foreign substrate coated by an adhesive layer (Intervia photodielectric 8023, ~4 μm). A spin-cast layer of polyimide (PI-2545, HD Microsystems, 3 μm) planarized the printed platforms. ICP-RIE (SF_6/O_2) exposed the electrodes for electrical measurements (*SI Appendix, Figure S3*), followed by subsequent metal interconnection. For the actively multiplexed array system, sputter-coated Cr/Au layers (AJA Sputtering system, 10/300 nm) served as electrical contacts as well as sensing pads interconnected to the electrodes of the microdie, as the first metal layer. A thin polyimide film (1.5 μm) with via openings and a second metal (Au) layer (electron-beam evaporation, 200 nm) yielded row select lines (*SI Appendix, Fig. S6*) and completed the fabrication process.

Preparation of PDMS Stamps. A spin-cast layer of a photodefinable epoxy (SU-8 50, MicroChem, 100 μm) on a Si wafer (100 mm diameter, University Wafer) served as the substrate for fabrication of molds for PDMS stamps. Photolithographically patterning the SU-8 layer yielded different patterns of openings to the underlying Si wafer. Drop casting a thick layer of PDMS (thickness of ~4 μm) on this structure, followed by curing at room temperature (~ 1 day) and then carefully peeling the PDMS layer from the SU-8/Si wafer substrate yielded the stamps, as shown in Fig. 2A.

Extraction of Transistor Parameters. The effective mobility (μ_{eff}) in the linear regime can be extracted using the following equation:

$$\mu_{eff} = \frac{\partial I_{DS}}{\partial V_{DS}} \cdot \frac{L}{WC_{OX}(V_{GS} - V_T - 0.5V_{DS})} \quad (\text{S1})$$

where V_T is the threshold voltage and C_{OX} is the specific capacitance of the gate per unit gating area, while the transistor gate area is $10 \times 33 \mu\text{m}$ ($L \times W$). The C_{OX} can be calculated via the following equation:

$$C_{OX} = \frac{\epsilon_0 \epsilon_r}{t_{OX}} \quad (\text{S2})$$

where the ϵ_0 is the permittivity (8.854×10^{-14} F/cm) and ϵ_r is the relative permittivity and t_{OX} is the oxide thickness. For the case of a gate dielectric of t-SiO₂ (50 nm thick) and Al₂O₃ (13 nm thick), the C_{OX} corresponds to a total value of $\sim 6.3 \times 10^{-8}$ F/cm². Here, the lateral diffusion of phosphorus during activation of oxidation process decreased the channel length (L , 10 μm) relative to its photolithographically defined value, thus yielding an effective channel length L_{eff} . The diffusion length (x_d) can be determined by the thermal process of phosphorus after doping, in which the thermal oxidation step for the gate oxide is 1,150 °C for 16 min. As calculated as $\sim 2 \mu\text{m}$ of x_d , the resulting value of L_{eff} yields as $\sim 6 \mu\text{m}$. As a result, the peak effective mobility in [SI Appendix, Fig. S3](#) is $\sim 600 \text{ cm}^2 (\text{V}\cdot\text{s})^{-1}$, which is consistent with previous reports (1).

Encapsulation Strategies with t-SiO₂ Barriers. Transfer printing delivered arrays of microdie onto a silicon wafer with a layer of thermal oxide on its surface (1 μm thick t-SiO₂ layer on 200 μm thick Si wafer). This t-SiO₂ layer served as the back-surface biofluid barrier. A second transferred t-SiO₂ layer served as the front-surface barrier. A coating of polyimide (1.5 μm) and a separate adhesive (Kwik-sil, World Precision Instruments, 13 μm) were formed on the second thermal oxide wafer. ICP-RIE (SF₆/O₂) removed the Si wafer and terminated at the back surface of the t-SiO₂, leaving a ~ 900 nm thick layer of t-SiO₂ as a transferred barrier ([SI Appendix, Fig. S15](#)) on the polyimide substrate, laminated on a temporary glass plate. A subsequent process bonded the front side of the printed microchip system with polyimide and Kwik-sil adhesive onto this preformed barrier structure. Similar

etching procedures removed the Si wafer. Peeling the system from the glass substrate yielded a piece of flexible electronics encapsulated on top and bottom by layers of t-SiO₂.

Procedures for Soak Testing of Microdie Devices. Soak tests involved electrical measurements of devices during continuous and complete immersion in PBS solution (pH of 7.4) at different temperatures. For tests on isolated, printed microdie or μ -ILEDs, a PDMS well structure confined the PBS solution within the central regions on the barrier layer over the test devices ($\sim 1 \text{ cm}^2$, and $\sim 2 \text{ cm}$ in depth of the well structure) to eliminate PBS penetration through the edges of the samples. Ultraviolet ozone (UVO) treatment of the surfaces of the barrier layers and the bottom surfaces of the PDMS well allowed strong bonding upon contact, thereby leading to a waterproof seal. Photolithographically patterned metallization (Cr/Au, 10/300 nm) served as electrical interconnects from the devices to probe pads outside the PDMS well, for subsequent measurements. For soak tests of the actively multiplexed systems, *in vitro* measurements involved complete, continuous immersion of the entire area of the array in PBS solution (Fig. 4C). Applying a combination of PDMS and KiwK-sil at the peripheral edges of the system minimized the effects of lateral water diffusion through polymer materials such as polyimide, bonding layers and interfaces.

Failure Mechanism Analysis for the Mg Structure. Soak tests of magnesium (Mg) thin films (200 nm, electron beam evaporation) encapsulated with t-SiO₂ revealed morphological information associated with water penetration. Here, the Mg electrode array adopted a geometry similar to that used for electrophysiological measurements, and served as a sensor of water penetration. The optical images in [SI Appendix, Fig. S5](#) show pristine Mg electrodes without any morphological change in the first 9 days of immersion but a rapid formation of Mg(OH)₂ defects afterward due to rapid bulk corrosion of Mg due to passage through the remaining t-SiO₂. The lifetime here (9 days) was consistent with that of single microdie (Fig. 3D). These results indicate that t-SiO₂ can offer excellent encapsulation capabilities for

printed electronic microsystems, where a slow hydrolytic reaction with water is responsible for the eventual failure ($\text{SiO}_2 + 2\text{H}_2\text{O} \rightarrow \text{Si}(\text{OH})_4$), as opposed to other mechanisms associated with pinhole defects or water permeation, consistent with a rate of ~ 100 nm/day in 96 °C PBS in previous reports (2).

Multiplexed Operation on a Representative Unit Cell: *SI Appendix, Fig. S7* displays the circuit diagram of the actively multiplexed addressing scheme, with a number of wires as 24. Two silicon transistors occupy each unit cell, where an amplifier transistor connected to sensing pads provided buffering of capacitive coupled bio-potentials, and the other transistor served as the multiplexer for an output signal to back-end DAQ system. The operation involved applied row voltages of + 2 V and -2 V to the gate electrode of the multiplexing transistor, to activate and inactivate a particular row, respectively. A constant current of 4 μA was applied to bias the column output and to form a common source follower. The entire device connected to the back-end DAQ system via a ZIF connector with 26 contacts. Similar principles of operation apply to previously reported systems (1).

DAQ Systems. As shown in *SI Appendix, Fig. S8*, the DAQ system included three PXI-6289 DAQ cards (National Instruments) and a custom acquisition system interface board. In this system, the ZIF (zero insertion force) connectors of the multiplexed array (**Fig. 4A**) connected to the DAQ system via two high-definition multimedia interface cables and an adaptor printed circuit board (*SI Appendix, Fig. S9*), where the connector of the array can be plugged or unplugged without damage. Custom LabVIEW software (National Instruments) controlled the DAQ system, to simulate bio-potentials. All recording used a sampling rate of 781.25 Hz per sensing site. An oversampling ratio of 16 further reduced the noise.

***In vitro* Experiments with an Active Matrix System.** The systems exhibited low mean channel noise of ~ 56 μV with good uniformity across the full array (*SI Appendix, Fig. S10*).

The total leakage current of the system remained as ~ 13 nA (*SI Appendix, Fig. S11*), well below the standard safety limit for biomedical implantable devices according to the International Organization for Standardization (ISO 14708-1:2014, 1 μ A). *SI Appendix, Fig. S12* illustrate the statistics of V_T and mobility for 10 different test transistors fabricated together with these active matrix arrays on the same platforms.

Calculation of the Concentration of Dissolved Si. Theoretical calculation revealed the time-dependent change in concentration dissolved elemental silicon from hydrolysis of the t-SiO₂. Accelerated soaking tests involved exposing the t-SiO₂ encapsulation layer (thickness of 900 nm and area of 1.05 \times 1.05 cm²) to 40 ml of PBS solution at 96 °C. We measured the dissolution rate of the encapsulation layer to be $r_{dis,SiO_2} = 100$ nm/day. Increases in the concentration of Si in the PBS solution before the t-SiO₂ layer is fully dissolved can be calculated as the following:

$$r_{ppm,Si} = r_{dis,SiO_2} \cdot A \cdot \rho_{t-SiO_2} \cdot \frac{M_{Si}}{M_{SiO_2}} \cdot \frac{1}{V} \approx 0.27 \text{ ppm/day} \quad (S3)$$

where A is the area of the t-SiO₂ encapsulant, ρ_{t-SiO_2} is the density of t-SiO₂ (3), M_{Si} and M_{SiO_2} are the molar mass of Si and t-SiO₂, and V is the volume of the PBS solution. The concentration of Si in the PBS solution increased linearly as a function of time and remained at a constant concentration after dissolution of the t-SiO₂ layer. The simulation result agrees well with the experimental measurement.

Simulation of Reactive Diffusion. A one-dimensional theoretical model has been established to investigate the reactive diffusion of water into a thin layer of t-SiO₂ with initial thickness h_{SiO_2} , where the origin is located at the bottom of t-SiO₂ and the y axis points upward in the thickness direction. In these experiments, a test structure that incorporates Mg films serves as a water penetration sensor, thus determining the system lifetimes. The governing reactive diffusion equation is (4)

$$D \frac{\partial^2 w}{\partial y^2} - kw = \frac{\partial w}{\partial t}, \quad 0 \leq y \leq h_{\text{SiO}_2}, \quad (\text{S4})$$

where w is the water concentration depending on position y and time t , D and k are the diffusivity of water and reaction constant between t-SiO₂ and water, respectively. With a constant water concentration w_0 ($=1 \text{ g cm}^{-3}$) at the top of t-SiO₂ and zero water flux at the bottom, we write the boundary conditions $w|_{y=h_{\text{SiO}_2}} = w_0$ and $\partial w/\partial y|_{y=0} = 0$. The initial condition of zero water concentration in t-SiO₂ gives $w|_{t=0} = 0$ ($0 \leq y < h_{\text{SiO}_2}$). By separation of variables, substituting $w = Y(y)T(t)$ into equation (S4) yields $DY''/Y - k = T'/T = -\lambda$, with λ being the eigenvalue. We thus have $Y = E \sin(\sqrt{(\lambda - k)/D}y) + F \cos(\sqrt{(\lambda - k)/D}y)$ and $T = e^{-\lambda t}$, with E and F being the constants to be determined from the homogeneous boundary conditions $w|_{y=h_{\text{SiO}_2}} = 0$ and $\partial w/\partial y|_{y=0} = 0$. These yield $Y|_{y=h_{\text{SiO}_2}} = 0$ and $\partial Y/\partial y|_{y=0} = 0$, therefore $E = 0$ and $\cos(\sqrt{(\lambda - k)/D}h_{\text{SiO}_2}) = 0$. We thus obtain a series of eigenvalues: $\lambda_n = k + D[(2n-1)\pi/(2h_{\text{SiO}_2})]^2$ ($n = 1, 2, 3, \dots$). The homogeneous solution of water concentration is thus obtained as $w_h = \sum_{n=1}^{\infty} \left\{ C_n \exp\left[-\left\{k + D\left[\frac{(2n-1)\pi}{2h_{\text{SiO}_2}}\right]^2\right\}t\right] \cos\left[\frac{(2n-1)\pi y}{2h_{\text{SiO}_2}}\right] \right\}$, with the constants C_n to be determined. By adding a particular solution $w_p = w_0 \cosh(\sqrt{k/D}y)/\cosh(\sqrt{k/D}h_{\text{SiO}_2})$ that satisfies the governing equation as well as $w_p|_{y=h_{\text{SiO}_2}} = w_0$ and $\partial w_p/\partial y|_{y=0} = 0$, the general solution is obtained as $w = w_h + w_p$. By the initial condition $w|_{t=0} = 0$, C_n is determined, and the final water concentration solution is

$$w = w_0 \left\{ \frac{\cosh\left(\sqrt{\frac{k}{D}}y\right)}{\cosh\left(\sqrt{\frac{k}{D}}h_{\text{SiO}_2}\right)} + \sum_{n=1}^{\infty} \frac{4(-1)^n (2n-1)\pi}{\frac{4kh_{\text{SiO}_2}^2}{D} + [(2n-1)\pi]^2} \exp\left\{-\left\{k + D\left[\frac{(2n-1)\pi}{2h_{\text{SiO}_2}}\right]^2\right\}t\right\} \cos\left[\frac{(2n-1)\pi y}{2h_{\text{SiO}_2}}\right] \right\} \quad (\text{S5})$$

SI Appendix, Fig. S14A shows the distribution of water concentration at different locations ($y = 850, 870, 890, \text{ and } 895 \text{ nm}$, respectively) of the 900-nm-thick t-SiO₂ barrier, which gradually increases with time and reaches saturation after around 10 hours in 96 °C PBS, revealing a fast equilibrium between reaction and diffusion. The steady-state limit of water concentration is determined from equation (S5) as $w|_{t \rightarrow \infty} = w_0 \cosh(\sqrt{k/D}y) / \cosh(\sqrt{k/D}h_{\text{SiO}_2})$. This saturated concentration shows an abrupt decrease from top to bottom of the t-SiO₂ barrier, reaching a very low level under the top surface, which indicates an effective delay of water permeation through t-SiO₂ (*SI Appendix, Fig. S14B*). The integration of $k w M_{\text{SiO}_2} h_{\text{SiO}_2} / (q \rho_{\text{SiO}_2} M_{\text{H}_2\text{O}})$ with respect to y and t gives the thickness of t-SiO₂ dissolved, where $q=2$ represents the number of water molecules that react with each atom of t-SiO₂ according to $\text{SiO}_2 + 2\text{H}_2\text{O} \rightarrow \text{Si}(\text{OH})_4$ (3), ρ_{SiO_2} is the mass density of t-SiO₂ ($=2.33 \text{ g cm}^{-3}$), M_{SiO_2} ($=60 \text{ g mol}^{-1}$) and $M_{\text{H}_2\text{O}}$ ($=18 \text{ g mol}^{-1}$) are the molar masses of t-SiO₂ and water, respectively. Equating the above dissolved thickness to h_{SiO_2} , the critical time for full dissolution of t-SiO₂, i.e., the lifetime of the test structure, can be solved. In this study, the effect of the summation in equation (S5) on the lifetime is negligible such that a simplified explicit expression of the lifetime is obtained:

$$t_{\text{critical}} = \frac{q h_{\text{SiO}_2} \rho_{\text{SiO}_2} M_{\text{H}_2\text{O}}}{w_0 M_{\text{SiO}_2} \sqrt{kD} \tanh\left(\sqrt{\frac{k}{D}} h_{\text{SiO}_2}\right)}. \quad (\text{S6})$$

The diffusivity D and reaction constant k at different temperatures can be extracted from the previous studies where the constants were determined based on the Arrhenius scaling and experimentally measured dissolution rates (2,5). For example, $D = 5.3 \times 10^{-20} \text{ cm}^2 \text{ s}^{-1}$, $k = 7.4 \times 10^{-8} \text{ s}^{-1}$ at 37 °C, and $D = 1.5 \times 10^{-16} \text{ cm}^2 \text{ s}^{-1}$, $k = 2 \times 10^{-4} \text{ s}^{-1}$ at 96 °C (5).

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Supplementary Figure Legends

Figure S1. Microdie array on wafer. (A) Optical microscope images of unit cells at various stages of fabrication of released microdie transistors, including Si doping, metal deposition and trench opening, from top to bottom, respectively. (B) Optical image of a large-scale array of microdie on a source wafer, which involves 10,000 microdie. Inset is an optical profilometry image of a representative unit cell after dry etching before TMAH undercut.

Figure S2. Schematic exploded-view illustration of the material stacks of a 4×4 array of NMOS transistors. The etched areas are bounded by Si (111) planes, with freely suspended devices tethered by SiN_x anchors across the trenches.

Figure S3. The performance of microdie before and after printing. (A) Linear and log scale transfer curves for a representative n-channel MOSFET on the source wafer (black) and after printing (blue). Inset is the process after printing, including polyimide planarization and opening of vias to the underlying electrodes by ICP-RIE. (B) Output characteristics after printing, for V_G from 0 to 5 V with 1 V steps.

Figure S4. Failure modes during printing process. (A) Crack failure. (B) Twist failure.

Figure S5. Left: Image of experimental setup for accelerated soak test in 96 °C PBS solution, pH 7.4. Right: Optical microscope images collected at several stages of accelerated aging test of the Mg system.

Figure S6. Microdie array fabrication. Optical microscope images of 4 unit cells at various stages of fabrication of Si transistors. PDMS stamps, sensing electrode pads, printing microdie arrays and multiplexing interconnect.

Figure S7. Schematic illustration of the capacitively coupled design of a 64-channel multiplexed device, showing the entire device (A) and a unit cell (B).

Figure S8. Schematic diagram of the DAQ system.

Figure S9. Photographs of an actively multiplexed system before (A) and after (B) the application of a Kapton stiffener (~0.2 mm thick), and after plugging into an adaptor PCB board through a ZIF connector (C, D).

Figure S10. Histogram of noise (with Gaussian line-shape fitting) measured from 64 channels of the device system.

Fig. S11. Leakage analysis of a representative actively multiplexed array. The total leakage current of the array is ~ 13 nA.

Figure S12. The performance of a test transistor in active multiplexed printed 8×8 microdie arrays. Statistics of test transistor peak effective mobility and V_T from 10 different arrays. Here the test transistors are fabricated together with the active matrix system on the same platform.

Figure S13. Histogram of device lifetimes (with Gaussian line-shape fitting) measured from 64 channels of the array system in accelerated soak tests in 96 °C PBS solution (pH 7.4). The unit cell failure is defined as the point when the pixelated gain value drops to 0.

Figure S14. Simulation results of water concentration. (A) Distribution of water concentration as a function of soaking time at different y positions through the SiO_2 . (B) Distribution of water concentration in 900-nm thick $t\text{-SiO}_2$ layer when saturation is reached after 10 hours.

Figure S15. The SEM image of a 900 nm thick layer of $t\text{-SiO}_2$ above the polyimide layer, as the biofluid barrier.

Figure S1

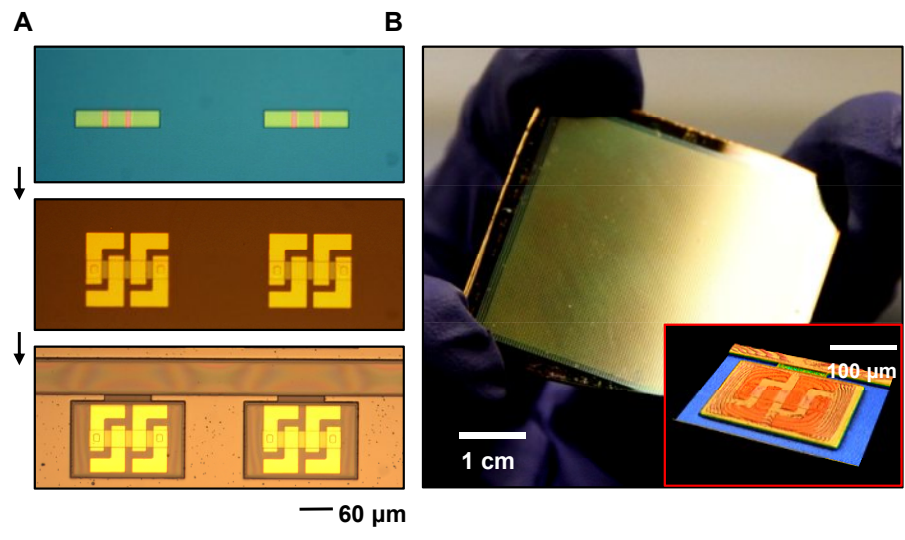


Figure S2

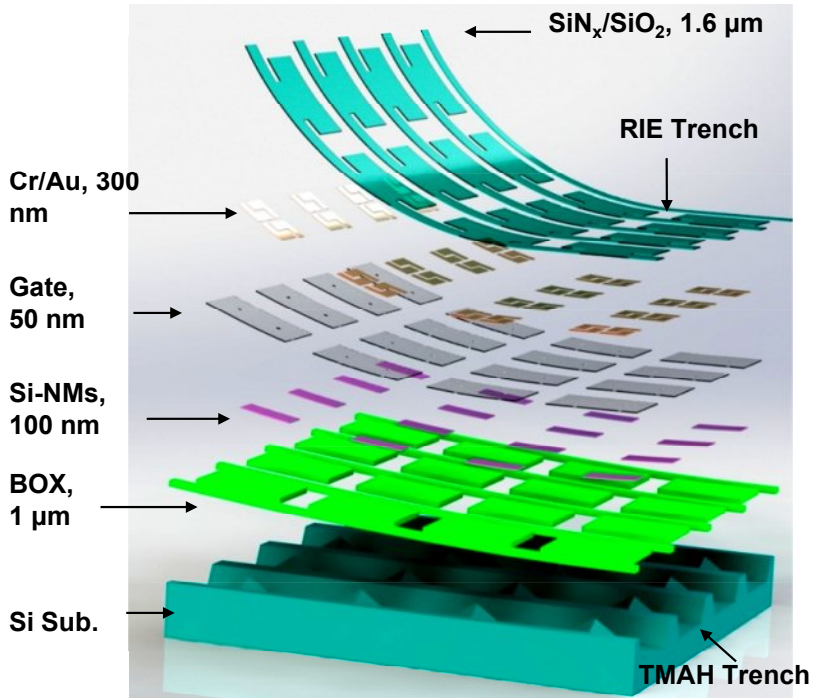


Figure S3

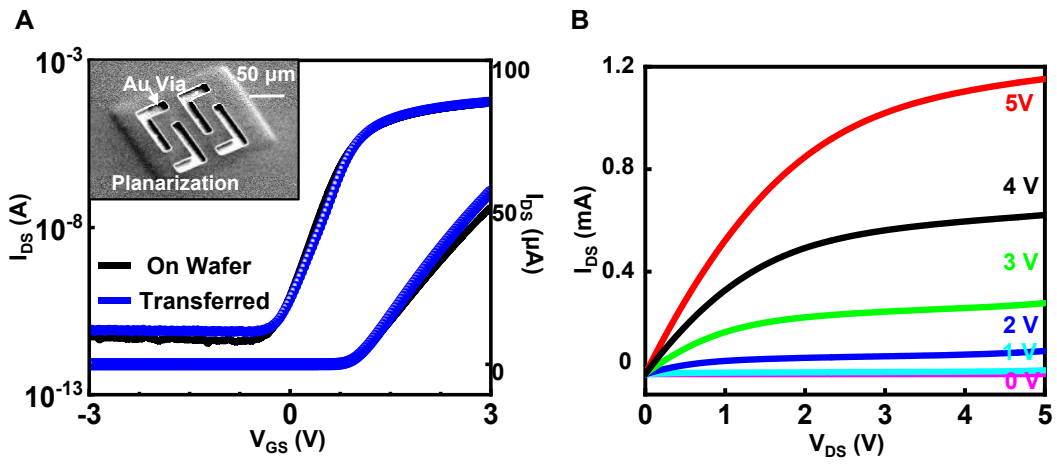


Figure S4

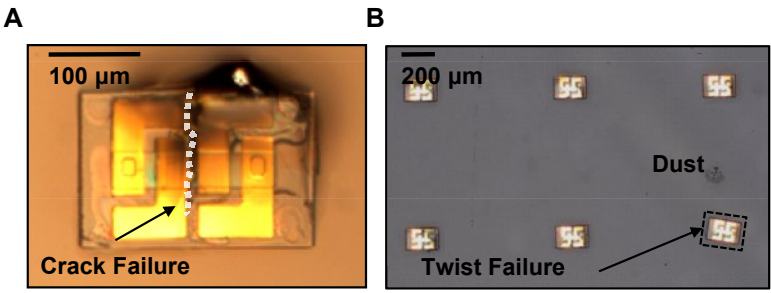


Figure S5

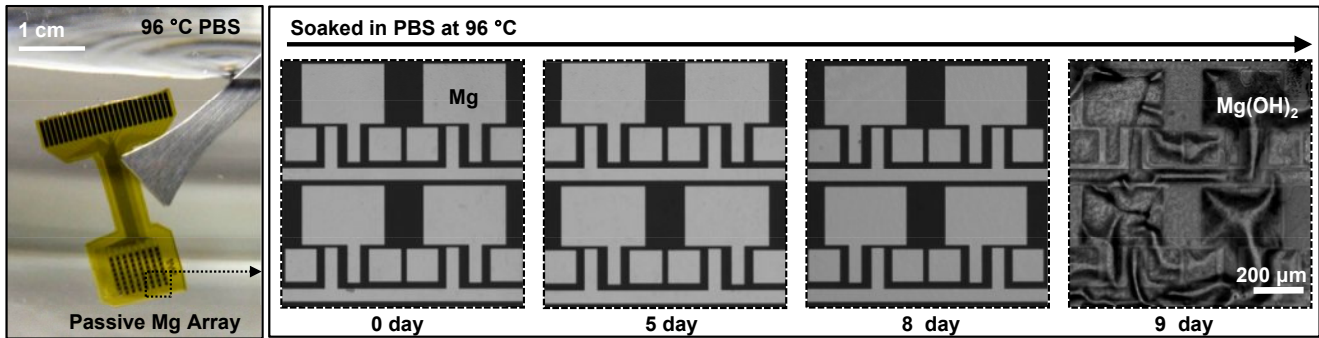


Figure S6

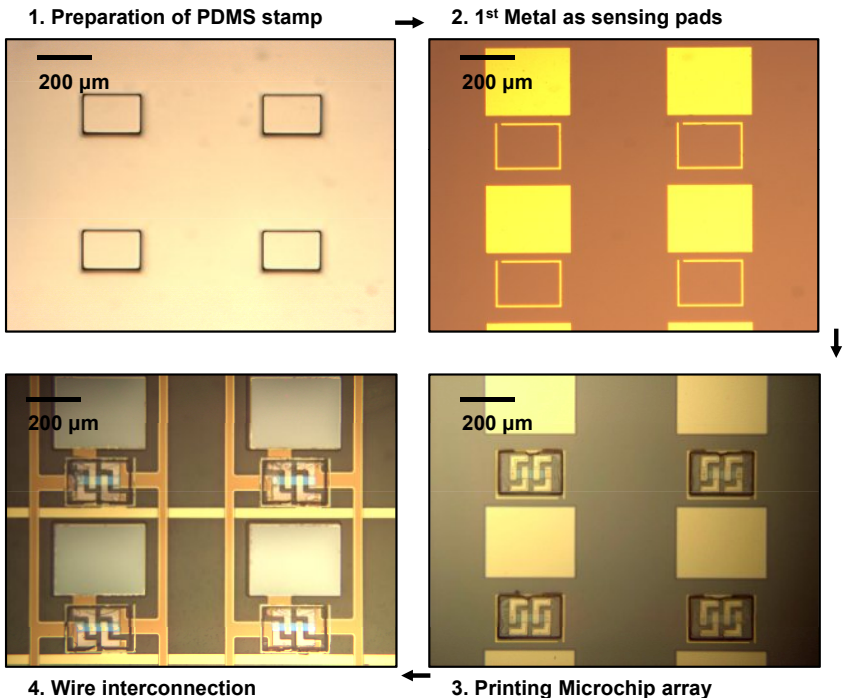


Figure S7

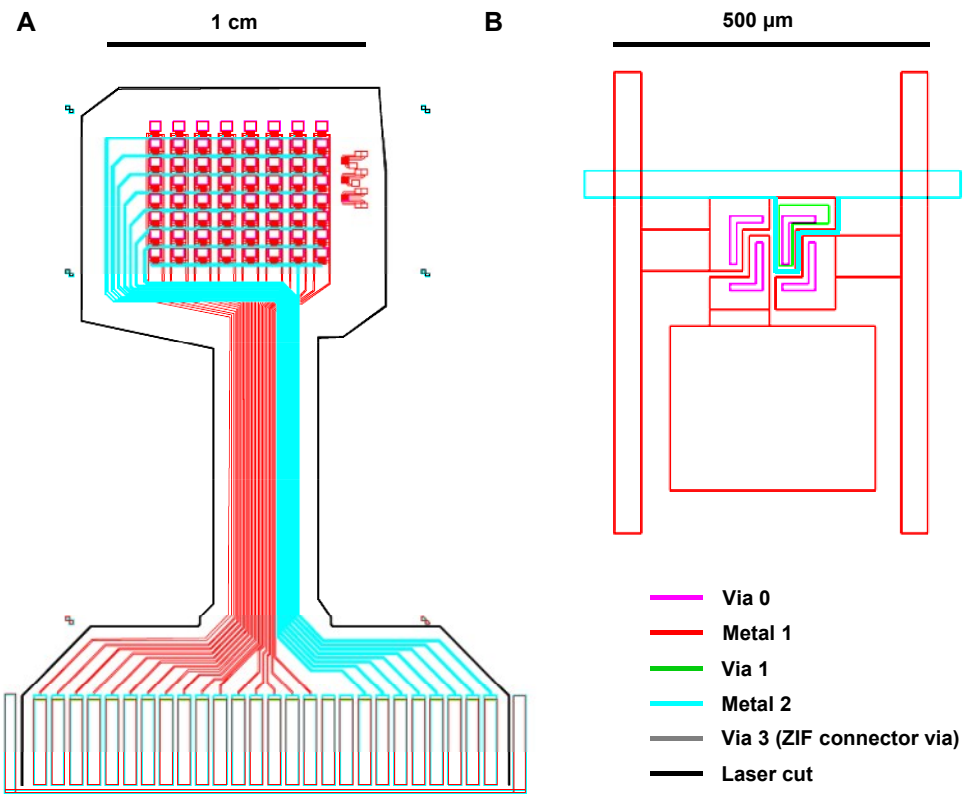


Figure S8

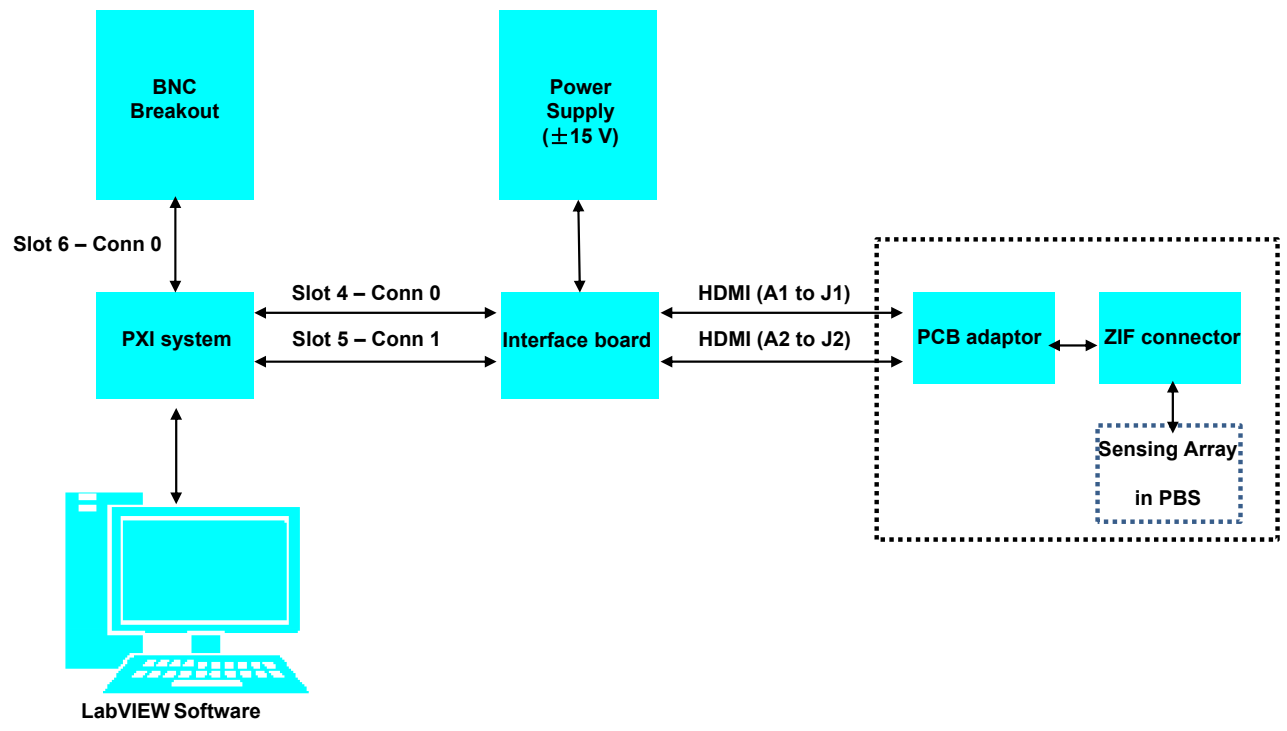


Figure S9

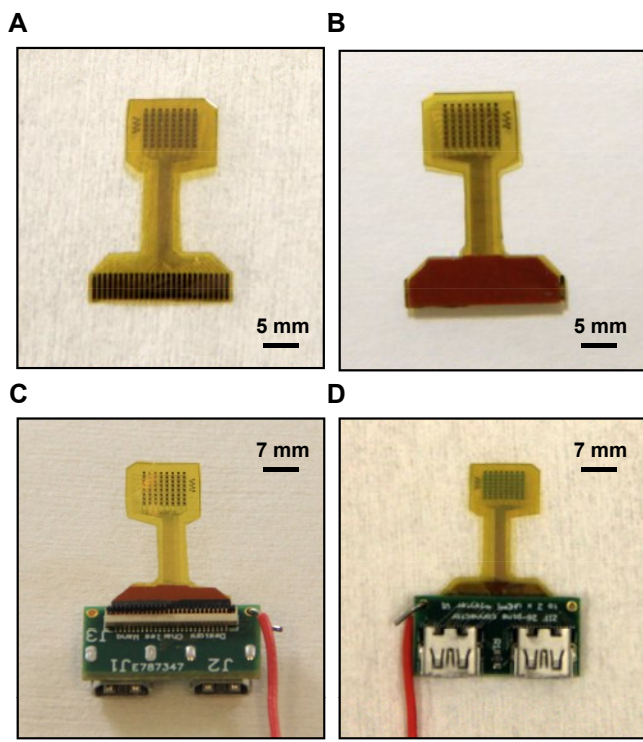


Figure S10

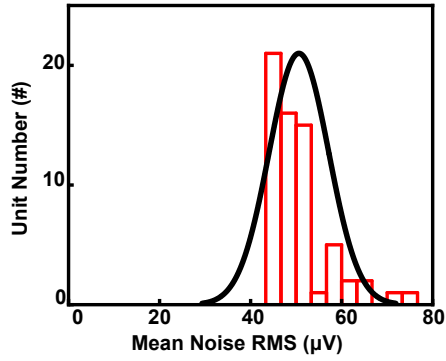


Figure S11

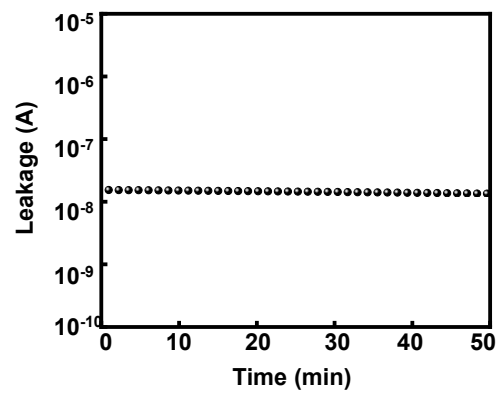


Figure S12

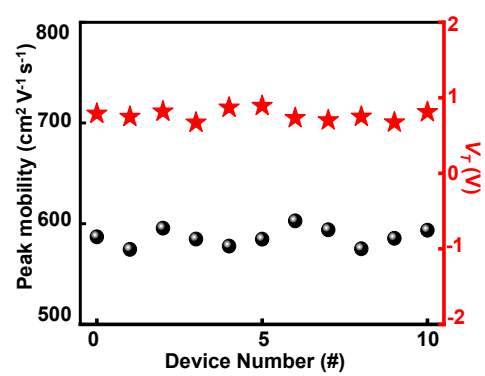


Figure S13

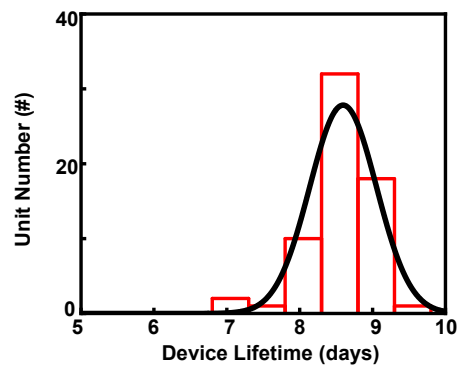


Figure S14

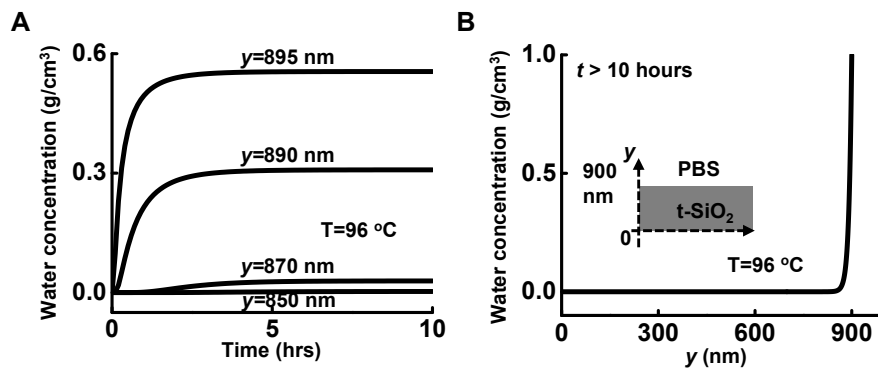


Figure S15

